105. In some implementations, the handheld device can be placed within an enclosure that can be worn on the head of the user. In some implementations, the HMD **120** is replaced with a CGR chamber, enclosure, or room configured to present CGR content in which the user does not wear or hold the HMD **120**.

[0030] FIG. **2** is a block diagram of an example of the controller **110** in accordance with some implementations. While certain specific features are illustrated, those skilled in the art will appreciate from the present disclosure that various other features have not been illustrated for the sake of brevity, and so as not to obscure more pertinent aspects of the implementations disclosed herein. To that end, as a non-limiting example, in some implementations the controller **110** includes one or more processing units **202** (e.g., microprocessors, application-specific integrated-circuits (ASICs), field-programmable gate arrays (FPGAs), graphics processing units (GPUs), central processing units (CPUs), processing cores, and/or the like), one or more input/output (I/O) devices **206**, one or more communication interfaces **208** (e.g., universal serial bus (USB), FIREWIRE, THUNDERBOLT, IEEE 802.3x, IEEE 802.11x, IEEE 802.16x, global system for mobile communications (GSM), code division multiple access (CDMA), time division multiple access (TDMA), global positioning system (GPS), infrared (IR), BLUETOOTH, ZIGBEE, and/or the like type interface), one or more programming (e.g., I/O) interfaces **210**, a memory **220**, and one or more communication buses **204** for interconnecting these and various other components.

[0031] In some implementations, the one or more communication buses **204** include circuitry that interconnects and controls communications between system components. In some implementations, the one or more I/O devices **206** include at least one of a keyboard, a mouse, a touchpad, a joystick, one or more microphones, one or more speakers, one or more image sensors, one or more displays, and/or the like.

[0032] The memory **220** includes high-speed random-access memory, such as dynamic random-access memory (DRAM), static random-access memory (SRAM), double-data-rate random-access memory (DDR RAM), or other random-access solid-state memory devices. In some implementations, the memory **220** includes non-volatile memory, such as one or more magnetic disk storage devices, optical disk storage devices, flash memory devices, or other non-volatile solid-state storage devices. The memory **220** optionally includes one or more storage devices remotely located from the one or more processing units **202**. The memory **220** comprises a non-transitory computer readable storage medium. In some implementations, the memory **220** or the non-transitory computer readable storage medium of the memory **220** stores the following programs, modules and data structures, or a subset thereof including an optional operating system **230** and a CGR experience module **240**.

[0033] The operating system **230** includes procedures for handling various basic system services and for performing hardware dependent tasks. In some implementations, the CGR experience module **240** is configured to manage and coordinate one or more CGR experiences for one or more users (e.g., a single CGR experience for one or more users, or multiple CGR experiences for respective groups of one or more users). To that end, in various implementations, the CGR experience module **240** includes a data obtaining unit **242**, a tracking unit **244**, a coordination unit **246**, and a data transmitting unit **248**.

[0034] In some implementations, the data obtaining unit **242** is configured to obtain data (e.g., presentation data, interaction data, sensor data, location data, etc.) from at least the HMD **120**. To that end, in various implementations, the data obtaining unit **242** includes instructions and/or logic therefor, and heuristics and metadata therefor.

[0035] In some implementations, the tracking unit **244** is configured to map the scene **105** and to track the position/location of at least the HMD **120** with respect to the scene **105**. To that end, in various implementations, the tracking unit **244** includes instructions and/or logic therefor, and heuristics and metadata therefor.

[0036] In some implementations, the coordination unit **246** is configured to manage and coordinate the CGR experience presented to the user by the HMD **120**. To that end, in various implementations, the coordination unit **246** includes instructions and/or logic therefor, and heuristics and metadata therefor.

[0037] In some implementations, the data transmitting unit **248** is configured to transmit data (e.g., presentation data, location data, etc.) to at least the HMD **120**. To that end, in various implementations, the data transmitting unit **248** includes instructions and/or logic therefor, and heuristics and metadata therefor.

[0038] Although the data obtaining unit **242**, the tracking unit **244**, the coordination unit **246**, and the data transmitting unit **248** are shown as residing on a single device (e.g., the controller **110**), it should be understood that in other implementations, any combination of the data obtaining unit **242**, the tracking unit **244**, the coordination unit **246**, and the data transmitting unit **248** may be located in separate computing devices.

[0039] Moreover, FIG. **2** is intended more as functional description of the various features that may be present in a particular implementation as opposed to a structural schematic of the implementations described herein. As recognized by those of ordinary skill in the art, items shown separately could be combined and some items could be separated. For example, some functional modules shown separately in FIG. **2** could be implemented in a single module and the various functions of single functional blocks could be implemented by one or more functional blocks in various implementations. The actual number of modules and the division of particular functions and how features are allocated among them will vary from one implementation to another and, in some implementations, depends in part on the particular combination of hardware, software, and/or firmware chosen for a particular implementation.

[0040] FIG. **3** is a block diagram of an example of the HMD **120** in accordance with some implementations. While certain specific features are illustrated, those skilled in the art will appreciate from the present disclosure that various other features have not been illustrated for the sake of brevity, and so as not to obscure more pertinent aspects of the implementations disclosed herein. To that end, as a non-limiting example, in some implementations the HMD **120** includes one or more processing units **302** (e.g., microprocessors, ASICs, FPGAs, GPUs, CPUs, processing cores, and/or the like), one or more input/output (I/O) devices and sensors **306**, one or more communication interfaces **308** (e.g., USB, FIREWIRE, THUNDERBOLT, IEEE 802.3x,